CLAIMS

1. An indium phosphide-based semiconductor double hetero-structure bipolar transistor comprising:

an emitter region having a first bandgap;

a base region in electrical communication with the emitter region, the base region having a second bandgap different from the first bandgap; and

a collector region containing indium and phosphorous and in electrical communication with the base and the emitter regions, the collector region having a third bandgap different from the second bandgap, the collector region containing at least three layers having different carrier concentrations.

2. The transistor as recited in claim 1, further comprising a sub-collector in electrical communication with the collector region, wherein the collector region comprises a first layer, a second layer adjacent to the first layer that has a lowest carrier concentration of the three layers, and a third layer adjacent to the second layer that has a highest carrier concentration of the three layers, and the first layer is closer to the sub-collector than either the second or third layers.

3. The transistor as recited in claim 2, wherein the second layer is an unintentionally doped layer.

4. The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the first layer to the second layer is at least about 3.

5. The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the third layer to the first layer is at least about 3.

6. The transistor as recited in claim 2, wherein a ratio of carrier concentrations of the third layer to the second layer is at least about 10.

7. The transistor as recited in claim 2, wherein the first layer is donor doped and has a carrier concentration of about 3E16 cm^{-3}.

8. The transistor as recited in claim 2, wherein the first layer is about 500 nm thick.

9. The transistor as recited in claim 2, wherein the second layer has a carrier concentration level at most about 1E16 cm^{-3}.

10. The transistor as recited in claim 2, wherein the second layer is about 250 nm thick.

11. The transistor as recited in claim 2, wherein the first layer has a substantially uniform carrier concentration.

12. The transistor as recited in claim 2, wherein the first layer has a graded carrier concentration that increases with increasing distance from the second layer.

13. The transistor as recited in claim 12, wherein the carrier concentration in the first layer is continuous across substantially the entirety of the first layer.

14. The transistor as recited in claim 2, wherein the collector region further comprises at least one additional layer disposed between the first layer and the sub-collector, a carrier concentration of the additional layer greater than the carrier concentration of the first layer.

15. The transistor as recited in claim 14, wherein a plurality of additional layers are disposed between the first layer and the sub-collector, carrier concentrations of the additional layers increasing with increasing distance from the first layer.

16. The transistor as recited in claim 15, wherein the carrier concentrations of the additional layers are substantially constant throughout each of the additional layers.

17. The transistor as recited in claim 15, wherein the carrier concentration of at least one of the additional layers is graded.

18. An indium phosphide-based semiconductor double heterostructure bipolar transistor comprising:

an emitter region having a first bandgap;

a base region in electrical communication with the emitter region, the base region having a second bandgap different from the first bandgap; and

a collector region in electrical communication with the base and emitter regions, the collector region having a third bandgap different from the second bandgap; and

a sub-collector in electrical communication with the collector region,

wherein the collector region contains indium and phosphorous, the collector region containing at least three layers having different conductivities.

19. The transistor as recited in claim 18, further comprising a sub-collector in electrical communication with the collector region, wherein the collector region comprises a first layer, a second layer adjacent to the first layer that has a lowest conductivity of the three layers, and a third layer adjacent to the second layer that has a highest conductivity of the three layers, and the first layer is closer to the sub-collector than either the second or third layers.

20. The transistor as recited in claim 19, wherein the second layer is an unintentionally doped layer.

21. The transistor as recited in claim 19, wherein the first layer is donor doped and has a carrier concentration of about 3E16 cm^{-3}.

22. The transistor as recited in claim 19, wherein the second layer has a carrier concentration at most about 2E16 cm^{-3}.

23. The transistor as recited in claim 19, wherein the first layer has a substantially uniform conductivity.

24. The transistor as recited in claim 19, wherein the first layer has a graded conductivity that increases with increasing distance from the second layer.

25. The transistor as recited in claim 24, wherein the conductivity in the first layer is continuous across substantially the entirety of the first layer.

26. The transistor as recited in claim 19, wherein the collector region further comprises at least one additional layer disposed between the first layer and the sub-collector, a conductivity of the additional layer greater than the conductivity of the first layer.

27. The transistor as recited in claim 26, wherein a plurality of additional layers are disposed between the first layer and the sub-collector, conductivities of the additional layers increasing with increasing distance from the first layer.

28. The transistor as recited in claim 27, wherein the conductivities of the additional layers are substantially constant throughout each of the additional layers.

29. The transistor as recited in claim 27, wherein the conductivity of at least one of the additional layers is graded.

30. A method of decreasing a knee voltage and decreasing an electric field at a collector-base junction of a double heterojunction bipolar transistor, the method comprising:

providing a sub-collector above a semi-insulating indium phosphide (InP) substrate;

providing a first collector layer above the sub-collector, the first collector layer containing n-type InP;

providing a second collector layer above the first collector layer, the second conductor layer containing unintentionally doped InP and having a carrier concentration at most about one third of a maximum carrier concentration of the first collector layer;

providing a third collector layer above the second collector layer, the third layer containing n-type InP having a carrier concentration at least about ten times that of the second collector layer;

providing a base region above the collector that is substantially lattice-matched to the third collector layer, the base region having a smaller energy gap than the third collector layer;

providing an emitter above the base region; and

providing a cap above the emitter region.

31. The method as recited in claim 30, wherein the first collector layer has substantially the same carrier concentration from an end closest to the sub-collector to an end most distal from the sub-collector.

32. The method as recited in claim 30, further comprising providing a transitional material between the third collector layer and the base region, the transitional material having a carrier concentration less than about 5E16 cm^{-3}.

33. A method of decreasing a knee voltage and decreasing an electric field at a collector-base junction of a double heterojunction bipolar transistor, the method comprising:

providing a sub-collector above a semi-insulating indium phosphide (InP) substrate;

providing an InP collector above the sub-collector, the collector having a region that is graded such that the region of the collector has a carrier concentration of at least about 1E17 cm^{-3} closest to the sub-collector and a carrier concentration of at most about 1E16 cm^{-3} most distal from the sub-collector;

providing a base region above the collector that is substantially lattice-matched to the collector, the base region having a smaller energy gap than the collector;

providing an emitter above the base region; and

providing a highly conductive cap above the emitter region.

34. The method as recited in claim 33, further comprising providing a section of the collector nearest the base region that has a carrier concentration substantially higher than the carrier concentration of the region of the collector most distal from the sub-collector.

35. The method as recited in claim 34, wherein the region of the collector is adjacent to the section of the collector.

36. The method as recited in claim 35, wherein the carrier concentration is substantially uniformly graded from an end of the region of the collector closest to the sub-collector to an end of the region of the collector adjacent to the section of the collector.

37. The method as recited in claim 33, wherein the region of the collector comprises a plurality of layers in which adjacent layers have decreasing carrier concentrations with increasing distance from the sub-collector.

38. The method as recited in claim 37, wherein the carrier concentrations in each of the plurality of layers is substantially uniform.

39. The method as recited in claim 33, further comprising providing an unintentionally doped transitional material between the collector and the base region, the transitional material containing InGaAsP.